JC760 U.S. PTO
10/01/4949
10/26/01

JC1039
JC5

U.S. UTILITY Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10014949	10/26/2001	257	25	2811	S RAO

**APPLICANTS: Yamamoto Makoto; Iwabuchi Akio;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
JAPAN P2001-128187 04/25/2001

PG-PUB DO NOT PUBLISH ☐ | RESCIND ☐

Foreign priority claimed ☐ yes ☐ no
35 USC 119 conditions met ☐ yes ☐ no
Verified and Acknowledged Examiners's initials

ATTORNEY DOCKET NO
44471-265522 (13700)

TITLE : Lateral transistor having graded base region, semiconductor integrated circuit and fabrication method thereof

U S DEPT OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
	Assistant Examiner	Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid	Primary Examiner	Sheets Drwg. / Figs.Drwg. / Print Fig.	Application Examiner
☐ TERMINAL DISCLAIMER	PREPARED FOR ISSUE		

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM
(Attached in pocket on right inside flap)